

Design of Digital Adder Using Reversible Logic

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ABSTRACT

Reversible logic circuits have promising applications in Quantum computing, Low power VLSI design, Nanotechnology, optical computing, DNA computing and Quantum dot cellular automata. In spite of them another main prominent application of reversible logic is Quantum computers where the quantum devices are essential which are ideally operated at ultra high speed with less power dissipation must be built from reversible logic components. This makes the reversible logic as a one of the most promising research areas in the past few decades. In VLSI design the delay is the one of the major issue along with area and power. This paper presents the implementation of Ripple Carry Adder (RCA) circuits using reversible logic gates are discussed.

Keywords - Reversible logic, Reversible logic circuits, Ultra high speed, Power dissipation, Ripple Carry Adder.

I. INTRODUCTION

One of the most interested topics in current researches of hardware designers is the low power circuit design. The one of the main concern in VLSI design is power dissipation. According to Moore's Law statement that the number of components on the chip will double for every 18 months. After studying the Moore's Law researchers have come to decide that as the number of components on the chip increases the power dissipation will also increase. In past different techniques were used to reduce power dissipation hence for VLSI designers the power minimization has become a prime factor. In recent times the one of the alternative technique to reduce power dissipation is reversible logic.

In year 1961 scientist R. Landauer demonstrated that the amount of energy dissipation is due to the loss of each bit information. The energy dissipation for one bit of information loss is the amount of $KT \ln 2$ joules, where K is the Boltzmann's constant and T is the Temperature at which operation is performed. The heat dissipated due to the loss of one bit of information is very small at room temperature, but in the case of high computational works when the numbers of bits are more the heat dissipated by them will be so large that it affects the performance and leads to the reduction of the lifetime of the components [1]. In 1973 C. H. Bennett illustrated that to avoid $KT \ln 2$ energy dissipation in a circuit, the logic circuit must be built with reversible logic gates [2].

Reversible computing is one of the innovative method in low power dissipating circuit design for cryptography, thermodynamics to reduce the power dissipation by eliminating information loss.

An adder is a digital circuit that performs addition of binary digit. Adder is the main component used in applications like Digital Signal Processor, Microprocessors etc. An Adder in which the carry-out of each full adder is the carry-in to the next most significant full adder, this type of adder is known as Ripple Carry Adder.

This paper shows the 16 bit reversible Ripple Carry Adders which are developed using two different reversible gates.

II. REVERSIBLE LOGIC GATES

A reversible logic gate is a logic circuit that has the N number of Inputs and N number of Outputs with a bijective mapping between the input and output vector. Thus an $N \times N$ reversible gate can be denoted as follows

$$I_v = (I_1, I_2, I_3, I_4, \dots, I_N) \text{ and } O_v = (O_1, O_2, O_3, O_4, \dots, O_N)$$

Where I_v and O_v represent the input and output vectors respectively.

To design a reversible circuits a set of reversible gates are needed which can generate a unique output vector for each given input vector, and vice-versa that is there is a one-to-one mapping between the input and the output vectors. Reversible logic circuits and arbitrary logic circuits are distinguished by two properties.

- (i) The number of output bits is equal to the number of input bits.
- (ii) For each input pattern maps to unique output pattern

From the view of reversible circuit design, the complexity and performance of circuit depends on the some of the following parameters.

Constant Inputs: The number of inputs to be maintained at 0 or 1 value in order to obtain the required function.

Garbage Output: The number of unused outputs which transforms the irreversible circuit into a reversible circuit.

Quantum Cost: Number of Primitive reversible logic gates required to realize the circuit.

There are various number of existing reversible gates. Some of them are discussed below.

2.1.1. Feynman Gate (FG)

Feynman gate is a 2 inputs 2 outputs (2x2) reversible gate. Another name for Feynman gate is Controlled-NOT gate having the mapping (A, B) to (P=A, Q=A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. This gate is useful for copying the required outputs. Therefore, it can be known as a copying gate. It has a quantum cost of one. Its logic circuit is shown in Fig 1 below.

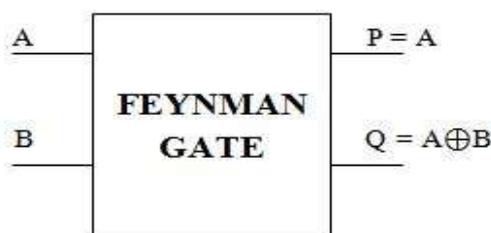


Fig 1: Feynman Gate

2.1.2. Fredkin Gate (FRG)

Fredkin gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A'B⊕AC, R=AB⊕A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It is also known as a Controlled Permutation gate. It has a quantum cost of five. Its logic circuit is shown in Fig 2 below.

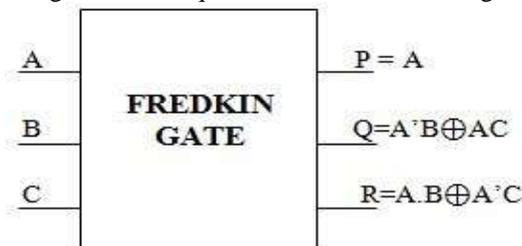


Fig 2: Fredkin Gate

2.1.3. Toffoli Gate (TG)

Toffoli Gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=B, R=A.B⊕C). The other name for Toffoli gate is controlled controlled-NOT gate. It has a quantum cost of five. Its logic circuit is shown in Fig 3 below.

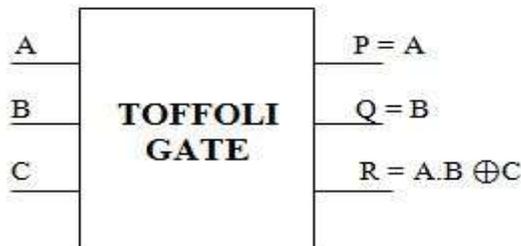


Fig 3: Toffoli Gate

2.1.4. Peres Gate (PG)

The Peres gate is a 3 inputs 3 outputs (3x3) reversible gate having the mapping (A, B, C) to (P=A, Q=A⊕B, R=(A.B)⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It's also known as the New Toffoli Gate (NTG). It is constructed by one Toffoli and one Feynman gate. It has a quantum cost of four. Its logic circuit is shown in Fig 4 below.

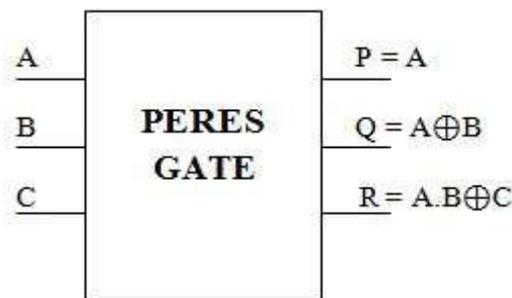


Fig 4: Peres Gate

2.1.5. HNG

The HNG is a 4 inputs 4 outputs (4x4) reversible gate having the mapping (A,B,C,D) to (P=A, Q=B, R= A⊕B⊕C, S = (A⊕B).C⊕AB⊕D)) where A,B,C,D are the inputs and P,Q,R,S are the outputs respectively. It has a quantum cost of six. Its logic circuit is shown in Fig 5 below.

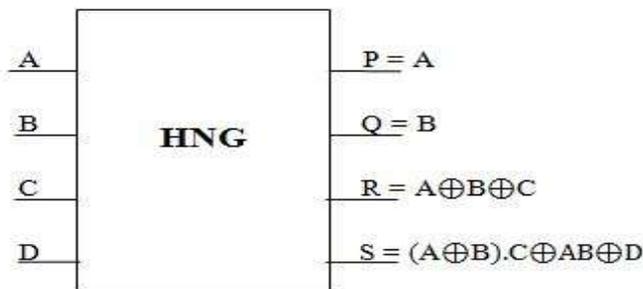


Fig 5: HNG

III. REVERSIBLE ADDERS

3.1 Reversible Full Adders

A Full adder is defined as circuit that takes two input bits, a carry-in bit and produces the output sum and carry out. Two types of reversible full adders are discussed here one is implemented with Peres gate and other one is using HNG.

The 3x3 Peres Gate is singly worked as half adder circuit when third input is set to zero i.e. third input is treated as a constant input. To implement the Reversible full adder circuit using Peres gate it requires two Peres gates which should be arranged as shown in Fig 6. Now this entire circuit is denoted as name Peres Full Adder Gate (PFAG). Peres Full Adder Gate produces two garbage outputs (g1 and g2), and requires one constant input. The constant input is set to zero to obtain the desired outputs.

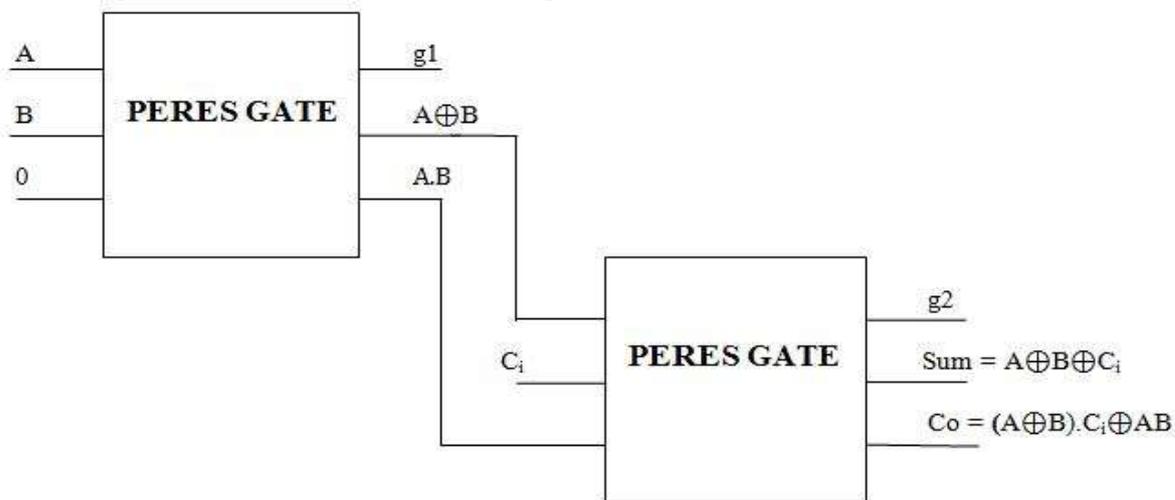


Fig 6: Peres Gates as Reversible Full Adder

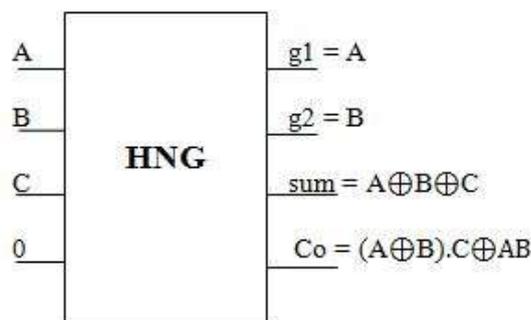


Fig 7: HNG Gate as Reversible Full Adder

Fig 7 shows that the HNG can singly worked as a Reversible Full Adder. To perform the operation as reversible full adder the fourth input of HNG should be treated as a constant input i.e. $D = 0$. The main difference between PFAG and HNG is two construct PFAG two Peres gates are needed each Peres gate quantum cost is 4 therefore PFAG total quantum cost is 8 where as HNG gate quantum cost is 6.

3.2 Ripple Carry Adder

The basic building block of the ripple carry adder is full adder. The binary full adder adds each input along with the applied carry in that is obtained as carry out from the addition of previous lower bits. To add two n bit binary numbers then n binary full adders should be interconnected. A Ripple carry adder is the inter connection of full adders.

The general output expressions for a ripple adder are

$$S_i = A \oplus B \oplus C_i$$

$$C_{i+1} = (A \oplus B) . C_i \oplus AB \quad (i=0, 1, 2, 3, 4, \dots)$$

The 16 bit ripple carry adder is obtained by cascading the 16 full adders in series. The block diagram of four bit ripple carry adder using Peres gate is shown in Fig 8.

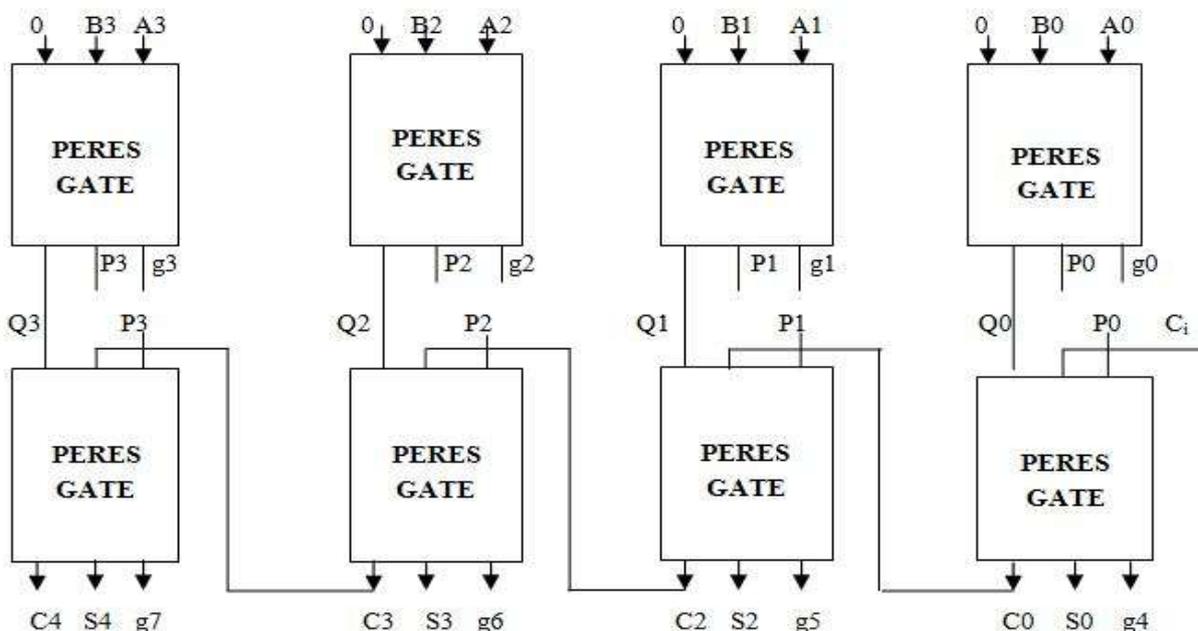


Fig 8: Reversible 4 bit PFAG Ripple Carry Adder

For implementing a four bit reversible ripple carry adder 8 Peres gates are needed. Hence the total gate count for four bit Ripple carry adder is 8. Therefore to construct a 16 bit ripple carry adder 32 Peres gates are required.

The block diagram of four bit ripple carry adder using HNG is shown in Fig 9. For constructing a four bit reversible ripple carry adder using HNG, 4 HNG are essential. Hence the total gate count for four bit Ripple carry adder is 4. Therefore to construct a 16 bit ripple carry adder 16 HNG are needed.

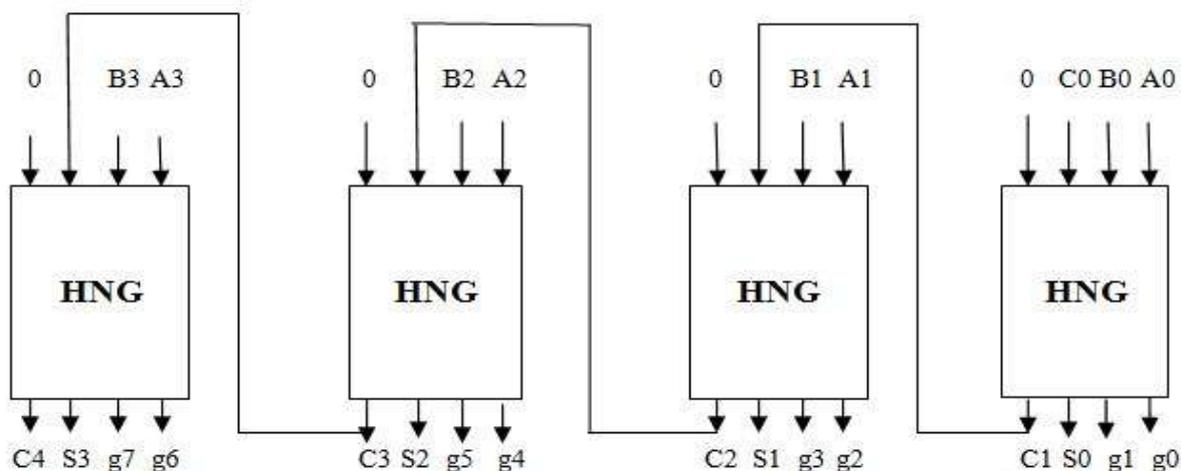


Fig 9: Reversible 4 bit HNG Ripple Carry Adder

IV. RESULTS

The above discussed Ripple carry adders are modelled using Verilog HDL. The functional verification is done and synthesized using Xilinx ISE.

TABLE 1: Comparison between Reversible Ripple Carry Adders

Parameters	16 bit Reversible Ripple Carry Adder using PFAG	16 bit Reversible Ripple Carry Adder using HNG
Gate count	32	16
Garbage output	32	32
Quantum cost	128	96

The comparison of two reversible Ripple Carry Adder based on three parameters i.e. Gate count, Garbage output and Quantum cost is shown in Table 1.

TABLE 2: Comparative results of conventional Ripple Carry Adder with Reversible Ripple Carry Adder

16 bit Ripple Carry Adders	Delay
Conventional Ripple Carry Adder	8.162ns
Reversible Ripple Carry Adder using PFAG.	7.798ns
Reversible Ripple Carry Adder using HNG	7.644ns

Table 2 shows the comparison of delay between the conventional and reversible Ripple Carry Adders.

V. CONCLUSION

In this paper, the reversible ripple carry adders, using PFAG and HNG are implemented. The performance of Ripple Carry Adder circuits can be improved using reversible logic and evaluate the number of gate count, garbage output, quantum cost and delay of the Ripple carry adders implemented using Reversible logic gates.

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